UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/075,113	02/13/2002	Marc Beaujoin	00GR227754352	6957

			EXAMINER
27975	7590	03/07/2006	TABONE JR, JOHN J

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ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 03/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/075,113	BEAUJOIN ET AL.
	Examiner	Art Unit	
	John J. Tabone, Jr.	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>27 December 2005</u>.

2a) ☒ This action is **FINAL.**   2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>9-31</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) <u>9,11,12,14-17,20-23 and 26-29</u> is/are rejected.

7) ☒ Claim(s) <u>10,13,18,19,24,25,30 and 31</u> is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on <u>13 February 2002</u> is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☒ All   b) ☐ Some * c) ☐ None of:

      1. ☒ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail. Date _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

FINAL DETAILED ACTION

1.   Claims 9-31 remain in the current application and have been examined.

Response to Arguments

2.   Applicants' arguments, see Appeal Brief, filed 12/27/2006, with respect to dependent claims 18, 24 and 30 and dependent claims 19, 25 and 31 have been fully considered and are persuasive. Therefore, the final rejection of these claims as set forth in the Final Office Action of 04/19/2005 has been withdrawn. However, Applicants' arguments concerning independent claims 9, 11, 14, 20 and 26 are not persuasive and the final rejection for these claims and their dependent claims, other than the above cited dependent claims, are maintained.

Arguments as per independent claims 9, 11, 14, 20 and 26:

The Applicants' arguments that the references fail to show certain features of applicant's invention can be summarized by the following: "*nothing in Marten et al. discloses testing a sequential access memory plane by extracting test words sequentially from the memory plane to compare with expected binary data bits, as claimed*". (Page 8, paragraph 3). The Examiner asserts that it is the combination of Kim et al. (hereinafter Kim) and Martens that teach the features of the Applicants' invention recited above. Kim teaches that the Output Data Evaluator (ODE) 120 is coupled to the output of the Data Output Register (DOR) 110 so as to receive the same data that is output to the Data Output (DO) line (extracting the p words from the data) and acts to

compact or otherwise optimize the data output from the DO line during test intervals based on responses generated by the RAM 102 to the test patterns provided by the TPG 118 (comparing the test bits of the extracted test words with expected data bits). (Col. 6, lines 23-49). Martens teaches that it is necessary to have the capability to read data out of the array serially (sequentially extracting test words) in certain chip-testing conditions. Martens teaches this capability, which is referred to as "scan testing" the array, requires that the array be able to hold its results in a group of memory elements where these memory elements are connected in series such that the output from the first memory element is fed to the scan input of the second element. Martens also teaches the output of the last memory element is fed to a test circuit outside the array (Kim's Output Data Evaluator (ODE) 120) for comparison to some expectation value. (Col. 5, lines 13-55, Fig. 4). The Examiner asserts that the combination of Martens' method of "scan testing" a memory array with Kim's extracting of test words and comparing them to expected values yields a memory array which is sequentially read and those outputs, being fed into the Kim's Output Data Evaluator (ODE) 120, are sequentially compared with expected values and would have been perfectly obvious to one of ordinary skill in the art at the time the invention was made. The Examiner would also like to point out the similarities between Applicants' Fig. 1 and Martens' Fig. 4 where elements 104, 102 and 103 of Martens' Fig. 4 correlates to BC0, BC1 and BC2 of Applicants' Fig. 1 for sequentially extracting the test words from the memory array.

Applicants state on page 9, paragraph 1, "*the Examiner is impermissibly using the teachings of Applicants' own patent application as a roadmap to modify the prior*

art". In response to Applicants' argument that the Examiner's conclusion of obviousness

is based upon improper hindsight reasoning, it must be recognized that any judgment

on obviousness is in a sense necessarily a reconstruction based upon hindsight

reasoning. But so long as it takes into account only knowledge which was within the

level of ordinary skill at the time the claimed invention was made, and does not include

knowledge gleaned only from the Applicants' disclosure, such a reconstruction is

proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). Further,

the Examiner contends that scannable memories are well known in the art for the

purpose of testing the memory and examining the contents. (See Stong et al. US-

6978406, Bui et al. US-6564344, Sanghani et al. US-6014762, US-6014762, US-

5881218, and Martens US-5751727). Martens, in particular suggests it would be

desirable to **improve the speed** of memory arrays utilized in high-speed ICs by utilizing

the scannable dynamic latch circuit. However, in doing so the best overall combination

of key criteria is realized: **minimum size, minimum delay,** and **proper testability** (i.e.,

scannability). (Col. 2, ll. 46-52, col. 8, ll. 47-52). The motivation to modify Kim's memory

is clearly stated in Martens and, as such, satisfies the "motivation to combine"

Applicants' arguments presented on pages 9-10.

Please note: For clarity the above presented motivation has been added to the

rejection of claims 9, 11, 14, 20 and 26, but by no means constitutes a new grounds for

rejection.

It is the Examiner's conclusion that independent claims 9, 11, 14, 20 and 26 are

not patentably distinct or non-obvious over the prior arts of record namely, Kim et al.

(US-6108802) in view of Martens (US-5751727). Therefore, the rejection is maintained.

Based on their dependency on claims 9, 11, 14, 20 and 26, claims 12, 15-17, 21-23 and

27-29, respectively, stand rejected. See Claims Objections for claims 10, 13, 18, 19, 24,

25, 30 and 31, below.

Claim Objections

3.   Claims 10, 13, 18, 19, 24, 25, 30 and 31 are objected to as being dependent

upon a rejected base claim, but would be allowable if rewritten in independent form

including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

4.   Claims 9, 11, 14-17, 20-23, 26-29 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Kim et al. (US-6108802), hereinafter Kim, in view of Martens (US-

5751727), hereinafter Martens.

Claims 9, 11, 14, 20 and 26:

Kim teaches a dual-port RAM-type FIFO memory device 100 (hereinafter

referred to as the FIFO 100) comprised of a Random Access Memory (RAM) 102 that

has n storage rows or words (shown in FIG. 3) where the input port 104 of the RAM 102

is connected to a Data Input Register (DIR) 108 and the output port 106 of the RAM 102

is connected to a Data Output Register (DOR) 110. Kim also teaches the FIFO 100

further includes a Write Address Register (WAR) 112 and a Read Address Register

(RAR) 114 where each register 112 and 114 is M-bits wide, where M is an integer equal

to the number of bits needed to address a RAM containing n words (a sequential

access memory array storing p words each of n bits). (Col. 4, lines 34-50). Kim further

teaches that BIST capability is provided by a BIST control 122 that controls a Test

Pattern Generator (TPG) 118, which generates test patterns in the form of vectors for

input to the RAM 102, and a Output Data Evaluator (ODE) 120. In addition, Kim teaches

during testing intervals, multiplexer 121 passes test patterns from the TPG 118 to the

DIR 108 for input to the RAM 102 (writing the memory array). Kim discloses that the

ODE 120 is coupled to the output of the DOR 110 so as to receive the same data that is

output to the Data Output (DO) line (extracting the p words from the data) and acts to

compact or otherwise optimize the data output from the DO line during test intervals

based on responses generated by the RAM 102 to the test patterns provided by the

TPG 118 (comparing the test bits of the extracted test words with expected data bits).

(Col. 6, lines 23-49). Kim does not explicitly teach the test words are "sequentially"

extracted or compared. However, Kim does teach the Output Data Evaluator (ODE) 120

is coupled to the output of the Data Output Register (DOR) 110 so as to receive the

same data that is output to the Data Output (DO) line (extracting the p words from the

data). Martens teaches that it is necessary to have the capability to read data out of the

array serially (sequentially extracting test words) in certain chip-testing conditions.

Martens teaches this capability, which is referred to as "scan testing" the array, requires

that the array be able to hold its results in a group of memory elements where these

memory elements are connected in series such that the output from the first memory

element is fed to the scan input of the second element. Martens also teaches the output

of the last memory element is fed to a test circuit outside the array (Kim's Output Data

Evaluator (ODE) 120) for comparison to some expectation value. (Col. 5, lines 13-55,

Fig. 4). It would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify Kim's Data Output Register (DOR) 110 with Martens'

scan register configuration shown in Figure 4. The artisan would have been motivated

to do so because it would enable Kim's Data Output Register (DOR) 110 to read data

out of the array serially (sequentially extracting test words) and subsequently Kim's

Output Data Evaluator (ODE) 120 will be able to compare the output test data

sequentially before extracting the next test word. The artisan also would have been

motivated to do so because Martens, in particular suggests it would be desirable to

improve the speed of memory arrays utilized in high-speed ICs by utilizing the

scannable dynamic latch circuit. However, in doing so the best overall combination of

key criteria is realized: **minimum size, minimum delay,** and **proper testability** (i.e.,

scannability). (Col. 2, II. 46-52, col. 8, II. 47-52).

Claims 15, 21,and 27:

Martens teaches latch output of column n is depicted at line 128 and scan output

n-1 is read to scan input n as depicted at line 132. (Col. 5, lines 51-53, Fig. 4). The first

and second control means disclose in the claimed invention is a typical capture (first

control means) and shift (second control means) procedure which is commonly used in

the art and would be obvious to one skilled in the art. The comparator means is taught

by Kim in the Output Data Evaluator (ODE) 120. (Col. 6, lines 23-49).

Claims 16, 22 and 28:

This claim is rejected per claims 14, 20 and 26 above. Also, Martens teaches that

the array scan latch organization of FIG. 4 includes multiple scannable latch circuits that

are coupled to one another. (Col. 6, lines 23-49).

Claims 17, 23 and 29:

Kim teaches that the ODE 120 is coupled to the output of the DOR 110 so as to

receive the same data that is output to the Data Output (DO) line (extracting the p words

from the data) and acts to compact or otherwise optimize the data output from the DO

line during test intervals based on responses generated by the RAM 102 to the test

patterns provided by the TPG 118 (comparing the test bits of the extracted test words

with expected data bits). (Col. 6, lines 23-49). Kim does not explicitly disclose that the

ODE 120 includes XOR and XNOR gates. However, Kim does teach the ODE 120

compacts or optimizes the data that is compared. It is well known in the art that this

procedure is accomplished through a XOR or XNOR logic and, therefore, is inherent in

Kim's ODE 120.

5.   Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et

al. (US-6108802), hereinafter Kim, in view of Martens (US-5751727), hereinafter

Martens, in further view of Zorian et al. (US-6330696), hereinafter Zorian.

Claim 12:

Kim does not explicitly teach the test words are written to obtain a checkerboard test pattern in the memory array. However, Kim does teach the RAM-type FIFO 100 may experience memory faults and functional faults associated with the RAM 102. (Col. 6, lines 66, 67, col. 7, line 1). Zorian teaches detection of junction leakage faults is accomplished by storing a pattern of alternating values in neighboring cells, such as storing a "checkerboard" pattern of"1"s and "0"s in the memory array. (Col. 4, lines 59-62, col. 6, lines 37-40, 46-51). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kim's fault detection algorithm to include Zorian's algorithm to detect junction leakage faults by writing a checkerboard pattern to the memory array. The artisan would have been motivated to do so because it would increase quality of the memory array test.

Allowable Subject Matter

6.   Claims 10, 13, 18, 19, 24, 25, 30 and 31 are allowed.

The following is an Examiner's Statement of Reasons for Allowance:

The present invention relates to sequential access memories, in particular first in/first out (FIFO) memories, and especially testing such memories, using a dedicated test circuit integrated during fabrication of the memory and the associated test algorithm.

The claimed invention as set forth in claim 10 (broadest claim) recites features such as: the p test words each of n bits are written in such a way as to obtain a

checkerboard test binary configuration in the memory array and sequentially obtaining

the expected data bits by respectively logically combining read addresses of the test

words and ranks of the test bits of each test word that is read.

The prior arts of record teach detection of junction leakage faults is accomplished

by storing a pattern of alternating values in neighboring cells, such as storing a

"checkerboard" pattern of"1"s and "0"s in the memory array; Zorian et al. (US-6330696)

is one example of such prior arts.

The prior arts of record, however, fail to teach, singly or in combination,

sequentially obtaining the expected data bits by respectively logically combining read

addresses of the test words and ranks of the test bits of each test word that is read. As

such, modification of the prior art of record to include the claimed *sequentially obtaining*

the expected data bits can only be motivated by hindsight reasoning, or by changing the

intended use and function of the prior art themselves. Therefore, it is not clear that one

of ordinary skill in the art at the time of the invention would have made the necessary

modifications to the prior art of record to encompass the *sequentially obtaining the*

expected data bits set forth in the present application. Moreover, none of the prior arts

of record, taken either alone or in combination, anticipate nor render obvious the

sequentially obtaining the expected data bits as set forth in claim 10. Dependent claims

13, 18, 24, and 30 also claim the *sequentially obtaining the expected data bits* limitation

are allowable for the same reasons as claim 10 above. Hence, claims 10, 13, 18, 19,

24, 25, 30 and 31 are allowable over the prior arts of record.

The Examiner agrees with the Applicant's arguments with regard to this feature in view of the arts of record; therefor, the Examiner favors the allowance of claims 10, 13, 18, 19, 24, 25, 30 and 31. Any comments considered necessary by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably accompany the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."
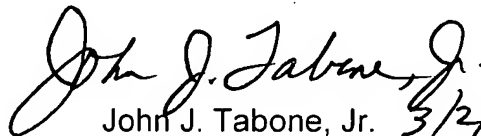
Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).
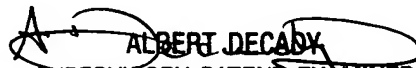
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number

for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the

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For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr.   3/2/06
Examiner
Art Unit 2133

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